REMARKS

The present response amends claim 5 to correct a dependency error. Claims 1, 2, 5-10, 12-16, and 18-20 are pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Petition under 37 C.F.R. § 1.181 Requesting Review of Prematurity of Final Rejection

Applicant hereby submits this petition and provisional response to the issues raised in the final Office Action. As noted in MPEP 706.07(c) and 1002.02(c), the finality of the previous Office Action is not subject to appeal and, therefore, it is appropriate to petition under 37 C.F.R. § 1.181(a)(1).

The finality of the final Office Action mailed February 3, 2004 was premature because it introduced a ground of rejection that was not present in the preceding Office Action. In addition, this new ground of rejection was not necessitated by any amendments of the claims nor based on information submitted in an Information Disclosure Statement filed in the period between the preceding Office Action and the final Office Action.

In the present case, the previous Office Action mailed August 13, 2003 deemed claims 4 and 11 as containing allowable subject matter. *See* Office Action mailed August 13, 2003, page 12. In response thereto, Applicant amended independent claims 1 and 10 with the allowable subject matter from claims 4 and 11, respectively. *See* Response to Office Action Mailed August 13, 2003, page 10. It was believed that independent claims 1 and 10 would now be allowed since claims 4 and 11 were previously searched and deemed allowable over the prior art. Applicant did not anticipate a new issue would develop with the newly cited reference to U.S. Patent No. 6,408,409 to Williams et al. (hereinafter "Williams").

It appears the Examiner has reversed his previous position that the subject matter of claims 1 and 10 (as amended with claims 4 and 11) are allowed, and for the first time has brought forth Williams. As set forth in MPEP 706.07:

> Before final rejection is in order a clear issue should be developed between the examiner and applicant. To bring the prosecution to as speedy conclusion as possible and at the same time to deal justly by both the applicant and the public, the invention as disclosed and claimed should be thoroughly searched in the first action and the references fully applied; and in reply to this action the applicant should amend with a view to avoiding all the grounds of rejection and objection. Switching . . . from one set of references to another by

> the examiner in rejecting in successive actions claims of substantially the same subject matter, will alike tend to defeat attaining the goal of reaching a clearly defined issue . . .

Applicant does not believe the mere placement of allowable subject matter into a claim necessitates the new grounds of rejection. Those grounds should have been made clear prior to the final rejection, and as a sense of equity, Applicant should be given the right to respond to Williams without the limitations of a final rejection being applied.

For at least the reasons set forth above, the finality of the Office Action mailed February 3, 2004 is asserted to be premature and erroneous, and Applicant respectfully requests its removal.

Objection to the Drawings

Applicant appreciates the Examiner's withdrawal of his objections to Figs. 1b and 2. However, it appears the Examiner has maintained his objection to Fig. 1a. Thus, the Examiner has requested that Fig. 1a be designated as "Prior Art." The Examiner references U.S. Patent Nos. 5,768,546 to Kwon (hereinafter "Kwon") and 5,748,947 to Fukushima (hereinafter "Fukushima") (final Office Action, page 2). For reasons set forth below, Applicant respectfully traverses this objection since neither Kwon nor Fukushima provide a figure that is "identical to" or "practically identical to" present Fig. 1a as alleged in the final Office Action.

First, with respect to Kwon, while item 42 of Fig. 1 indicates a FIFO buffer memory, a closer examination of the relevant passage of Kwon indicates data word 62 is not the same as the data D bits of present Fig. 1a (Kwon -- col. 1, lines 31-41). Specifically, each square designated as, for example, "V0," "X," etc. is a byte and each data word 62 constitutes four bytes (Kwon -- col. 1, lines 38-40). Comparing the present Fig. 1a, it is clear that each square (for example, $d_{6,0}$) is a bit -- not a byte, and each of the N entries need not constitute a four-byte data word as required in Kwon.

Second, with respect to Fukushima, Fig. 5 in no way describes an entry, or any form of correlation, between the tag bits and data bits shown (Fukushima -- Fig. 5). Specifically, Fukushima makes clear that the tag bits and data bits coming from FIFO 4 are dispatched in parallel, with the data bits coming subsequent to the tag bits (Fukushima -- col. 5, lines 50-53). Thus, unlike the N entries of present Fig. 1a with relationships drawn between, for example, $d_{0,0}$-$d_{0,7}$ data bits and $t_{0,0}$-$t_{0,3}$ tag bits, there

appears no relationship in Fukushima of the data bits and tag bits in Fig. 5 therein, other than the data bits (possibly not those shown) come subsequent to the tag bits.

Therefore, Applicant believes that present Fig. 1a must be read in the context of the present application. When doing so, the illustration as well as the description of Fig. 1a must be compared against the cited art. When placed in that context and when reviewing the description of the relevant drawings of the cited art, it appears that any commonality to present Fig. 1a rapidly disappears. Thus, Applicant respectfully traverses the Examiner's request that Fig. 1a be labeled as "Prior Art."

Claim Objections

Applicant appreciates the Examiner's withdrawal of claim objections of claims 10 and 18.

Section 112 Rejection

The Examiner has rejected claims 5-9 under 35 U.S.C. § 112, second paragraph. In response thereto, Applicants acknowledge a typographical error in claim 5 and have amended claim 5 to correct the error. Applicant appreciates the Examiner's thorough examination of claim dependency in bringing this error to Applicant's attention.

Section 103 Rejection

Claims 1, 2, 5, 6, 10, 12, 13, and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams in view of the Applicant's admitted prior art (hereinafter "APA"). To establish a case of *prima facie* obviousness of a claimed invention, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Second, there must be a reasonable expectation of success. As stated in MPEP 2143.01, the fact that references can be hypothetically combined or modified is not sufficient to establish a *prima facie* case of obviousness. *See In re Mills*, 916 F.2d. 680 (Fed. Cir. 1990). Finally, the prior art references must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d. 981 (CCPA 1974); MPEP 2143.03, emphasis added. Specifically, "all words in a claim must be considered when judging the patentability of that claim against the prior art." *In re Wilson* 424 F.2d., 1382 (CCPA 1970). Using these standards, Applicants contend that the

cited art fails to teach or suggest all features of the currently pending claims, some distinctive features of which are set forth in more detail below.

The cited art does not teach or suggest, either singularly or in combination: (i) which storage location, of the N storage locations has been written to in lieu of being read from (claim 1); or (ii) which FIFO location has been written to and which location has been read (claim 10). Present independent claims 1 and 10 each recite a mechanism by which the write and read statuses of various locations can be determined. Specifically, claim 1 recites a logic gate associated with each of the N storage locations. The logic gate can compare a particular bit in a write register with a particular bit in a read register to determine, for that storage location having those corresponding bits, whether that storage location has been written to or read from. Claim 10 makes clear that the read and write registers record which, from among many, FIFO location has been written to and which has been read from. Thus, claims 1 and 10 define a mechanism for noticing for each entry whether that entry has been written to or read from.

Contrary to keeping track of the read/write statuses of each entry, Williams simply keeps track of the overflow or underflow conditions that might exist within a buffer (Williams -- col. 1, lines 61-63). The underflow or overflow conditions are noted by reading a count value (from 0 to 8) within read and write counters 230 and 240, respectively (Williams -- col. 4, lines 23-29; Fig. 2). As data is, for example, read from the buffer 108, the number of read counts from counter 240 is used to toggle flip-flop 244 once comparison circuit 242 achieves, for example, an underflow status (i.e., an 8 count has occurred) (Williams -- col. 4, lines 44-54; Fig. 2). A flow error 248 will be noted if an underflow condition is set by flip-flop 244 when a data word is attempted to be read from port 105 of buffer 108. This is achieved by forwarding the corresponding flow indicator bit 220-228 to the input of logic gate 246, along with the underflow condition output from flip-flop 244 (Williams -- col. 4, lines 55-67; Fig. 2).

Thus, while Williams appears to keep track of, for example, an underflow condition to note that subsequent read data is invalid, Williams does not teach or suggest a logic gate that keeps track of, for each entry of the N storage locations, which of the N storage locations have been written to in lieu of being read from (claim 1), or that there are read and write registers that record which locations have been written to and read from (claim 10). Simply put, Williams only counts the number of entries read into and read from FIFO 108 via counters 230-240, but does not note which of the various data words 210-218 have been written to in lieu of being read from, as presently claimed.

The cited art does not teach or suggest a logic gate associated with each storage location (claim 1). As recognized on page 4 of the final Office Action, "Williams does not specifically show a logic gate that is associated with each of the storage locations . . ." Yet, however, the Examiner argues that decision block 526 of Fig. 5B in Williams somehow alludes to or suggests to one of ordinary skill in the art, without undue experimentation, that the use of a logic gate as claimed would be obvious. Applicant respectfully disagrees. The decision block 526 of Fig. 5B in Williams has nothing whatsoever to do with keeping track of which storage location has been written to in lieu of being read from, much less somehow implying a logic gate for that purpose.

A closer reading of Williams will illuminate the true meaning of decision block 526. Specifically, step 526 is simply a step that causes the system to "loop" and thereby wait until it is time to read data from the ring buffer 108 (Williams -- col. 7, lines 56-58). Nowhere in the passage which describes step 526 is there any explicit or implicit teaching that would motivate one skilled in the art, upon reviewing Williams, to somehow deduce that essentially a wait state would spark a thought that a claimed logic gate could be used to keep track of, for corresponding storage locations, which location has been written to in lieu of being read from. There simply is no passage within Williams that makes the leap alleged by the Examiner. In fact, a close reading of Williams indicates that no mechanism is in place to record which storage location contains read data or written data -- Williams simply counts entries stored and entries read to determine whether or not an overflow or underflow condition exists. This is certainly different from, and no way suggests, the claimed logic gate which serves the function set forth in claim 1.

The cited art does not teach or suggest tag bits used to determine the status of certain N storage locations written to in lieu of being read from. Present claims 1 and 10 each recite the use of tag bits. More importantly, each such claim uses tag bits for a particular purpose. Namely, the tag bits will determine which of the various FIFO locations have been written to in lieu of being read from. *See*, for example, the last element of claim 10. Applicant agrees with the Examiner in that "Williams does not teach associated tag bits with each data entry." (Final Office Action, page 5) However, Applicant must disagree that Williams, which does not mention anywhere the use of tag bits, can somehow be combined with the use of tag bits in general to denote a type of transaction. Nowhere in the APA is there any mention that tag bits can be used to determine the status of storage locations that have been written to in lieu of being read from, as presently claimed. Instead, the APA only mentions that tag bits "may be used

as flags to denote a type of transaction for which the data is intended." Such an example might be transactions to peripheral devices as opposed to memory.

Absent any mention of tag bits in Williams and absent any mention of tag bits used to determine read and write status, Applicant believes it is inappropriate to make the hypothetical combination suggested in the final Office Action, pages 5-6. There must be some suggestion in the cited art that would lead a skilled artisan to make this combination and, absent any relevant use of tag bits to the present claims, a skilled artisan simply cannot make the combination suggested in the final Office Action.

For at least the reasons stated above, Applicant believes that independent claims 1 and 10, as well as claims dependent therefrom, are patentable over the cited art. Accordingly, Applicant respectfully requests removal of this rejection.

Allowable Subject Matter

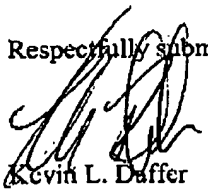
Applicant appreciates the Examiner's indication that claims 7-9 and 15-20 are allowable. However, in light of the above remarks, Applicant believes all the currently pending claims are allowable.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the final Office Action mailed February 3, 2004. In view of remarks traversing the objections and rejections, Applicants assert that pending claims 1, 2, 5-10, 12-16, and 18-20 are in condition for allowance. If the Examiner has any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment. However, if a fee is required for the petition contained herein, the Commissioner is authorized to charge LSI Logic Corporation Deposit Account No. 12-2252/00-309.

Respectfully submitted,



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